## REMARKS

*Double Patenting Rejection*

Claims 1-10 and 16-20 were provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-21 of copending U.S. Patent Application Serial No. 09/943,476, in view of *Dye* (U. S. Patent No. 6,145,069).

While Applicant still believes that the claims of the present invention are a non-obvious variation of the claims of the co-pending application SN 09/943,476, a terminal disclaimer has been included with this response in the interest of expediency.

*Claim Rejections Under 35 U.S.C. § 102*

Claims 1 and 3-5 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Dye*. Applicant respectfully traverses this rejection.

*Dye* discloses a flash memory system 900, with a decompression engine 280, that is coupled to a micro processing unit 400 and SRAM or DRAM main memory 440 over a system bus 118. *Dye* neither teaches nor suggests a non-volatile memory with a decompression capability that transfers data over a dedicated bus between the memories without intervention from another device, as claimed by Applicant.

*Claim Rejections Under 35 U.S.C. § 103*

Claims 2, 5-7, 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dye* in view of *Harari et al.* (U.S. Patent No. 6,266,724), and further in view of *Fallon et al.* (U. S. Patent Application Publication 2002/0069354A1). Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Iverson* (U.S. Patent No. 6,332,172). Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of *Iverson* and further in view of *Harari et al.* Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dye*, *Harari et al.*, and *Fallon et al.*, and further in view of *Baltz et al.* Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.*, *Iverson* and *Harari et al.* as applied to claim 16 above, and further in view of *Shin* (U.S. Patent No. 6,735,669).

*Baltz et al.* discloses using DMA circuitry 100 to transfer data from an 8-bit EPROM 671 to internal program memory 23 as is illustrated in Figure 8. Applicant's invention, as claimed in

the amended claims, does not require such intervention. Decompressed data from the non-volatile memory is transferred over a dedicated bus to volatile memory independent of the processor or DMA circuitry. Therefore, Applicant's invention as claimed is neither taught nor suggested by *Baltz et al.*

*Harari et al.* discloses a mother card 10 that includes a controller 41 and functional modules 42. Two of the possible functions of these modules 42 are the compression and decompression of data. A daughter card 20 can carry memory for the system. *Harari et al.* neither teaches nor suggests Applicant's invention of the non-volatile memory decompressing and transferring data to the volatile memory over a dedicated bus without intervention.

*Iverson* discloses a method for virtual memory compression in which a compressed image is stored in flash memory. *Iverson* neither teaches nor suggests Applicant's invention of a non-volatile memory decompressing stored compressed data as it is being transferred out to volatile memory over a dedicated bus without intervention.

*Fallon et al.* discloses methods and systems for accelerated loading of operating systems. None of the systems disclose or suggest a non-volatile memory with a decompression algorithm that transfers decompressed data over a dedicated bus to a volatile memory without intervention, as claimed by Applicant.

*Shin* discloses a Rambus RAM that has various modes for low power system operation. *Shin* neither teaches nor suggests Applicant's invention as claimed in the amended claims.

Even if it were obvious to combine *Dye*, *Harari et al.*, *Fallon et al.*, *Baltz et al.* and/or *Shin* in any combination, and Applicant maintains that it is not, no combination of the references can teach or suggest Applicant's invention. None of the references teach or suggest Applicant's invention as claimed in the amended claims for storing compressed data from a processor in a non-volatile memory having a decompression capability that decompresses the data as it is being transferred, without intervention, to a volatile memory over a dedicated bus.

## CONCLUSION

Applicant respectfully requests that the Examiner enter the present amendment, withdraw the final rejection, and allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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